

CLAIMS

1. An apparatus for phase and frequency locking, comprising:

a voltage controlled Phased Locked Loop (PLL), wherein  
5 the PLL is at least configured to have a Low Pass Filter (LPF) and a Voltage Controlled Oscillator coupled at a first node; and

a charge leakage correction circuit at least coupled to the first node.

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2. The apparatus of Claim 2, wherein the charge leakage correction circuit further comprises:

a charge pump, wherein the charge pump is at least configured to add charge to the LPF and wherein the charge  
15 pump is at least configured to subtract voltage from the LPF; and

a differentiator, wherein the differentiator is at least coupled to the charge pump and wherein the differentiator is at least configured to measure the rate of  
20 change of the across the LPF.

3. An apparatus for phase and frequency locking, comprising:

a voltage controlled Phased Locked Loop (PLL), wherein  
25 the PLL is at least configured to have a Low Pass Filter

(LPF) and a Voltage Controlled Oscillator coupled at a first node; and

5 a charge leakage correction circuit at least coupled to the first node, wherein the charge leakage correction circuit further comprises:

a charge pump, wherein the charge pump is at least configured to add charge to the LPF and wherein the charge pump is at least configured to subtract voltage from the LPF; and

10 a differentiator, wherein the differentiator is at least coupled to the charge pump and is at least configured to be coupled to the first node, and wherein the differentiator is at least configured to measure the rate of change of the voltage across the LPF.

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4. The apparatus of Claim 3, wherein the charge pump further comprises:

a plurality of switches at least configured to be coupled to the first node;

20 a positive current source coupled to at least one first switch of a plurality of switches; and

a negative current source coupled to at least one second switch of a plurality of switches.

5. The apparatus for correcting charge leakage across an LPF, comprising:

a charge pump, wherein the charge pump is at least configured to add charge to the LPF and wherein the charge 5 pump is at least configured to subtract voltage from the LPF; and

a differentiator, wherein the differentiator is at least coupled to the charge pump and is at least configured to be coupled to the first node, and wherein the 10 differentiator is at least configured to measure the rate of change of the voltage across the LPF.

6. A method for correcting charge in a PLL having an LPF, comprising:

15 locking a phase and a frequency;  
measuring the rate of change for voltage across the LPF  
if the rate of change of voltage across the LPF is  
positive, removing charge from the LPF; and  
if the rate of change of voltage across the LPF is  
20 negative, adding charge to the LPF.

7. A method for correcting charge in a PLL having an LPF, comprising:

locking a phase and a frequency;

measuring the voltage across the LPF at lock to obtain a first measured voltage;

measuring the voltage across the LPF periodically after lock to obtain a second measured voltage;

5 if difference between the second measured voltage and the first measured voltage is positive, removing charge from the LPF;

if difference between the second measured voltage and the first measured voltage is positive, adding charge to the  
10 LPF.

8. A computer program product for correcting charge in a PLL having an LPF, the computer program having a medium with a computer program embodied thereon, the computer  
15 program comprising:

computer program code for locking a phase and a frequency;

computer program code for measuring the rate of change for voltage across the LPF

20 if the rate of change of voltage across the LPF is positive, computer program code for removing charge from the LPF; and

if the rate of change of voltage across the LPF is negative, computer program code for adding charge to the  
25 LPF.

9. A computer program product for correcting charge in a PLL having an LPF, the computer program having a medium with a computer program embodied thereon, the computer 5 program comprising:

computer program code for locking a phase and a frequency;

computer program code for measuring the voltage across the LPF at lock to obtain a first measured voltage;

10 computer program code for measuring the voltage across the LPF periodically after lock to obtain a second measured voltage;

if difference between the second measured voltage and the first measured voltage is positive, computer program 15 code for removing charge from the LPF;

if difference between the second measured voltage and the first measured voltage is positive, computer program code for adding charge to the LPF.